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EXAMINER	
YU, HENRY W	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/613,897	BOESEL ET AL.	
	Examiner	Art Unit	
	HENRY YU	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

INFORMATION CONCERNING RESPONSES

Response to Amendment

1. This Office Action is in response to applicant's communication filed December 20, 2007, in response to PTO Office Action mailed June 22, 2007. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, **claims 1, 3, 9-11, 13, 17-18, and 22** have been amended. As a result, **claims 1-22** are now pending in this application.

3. The objections to the drawings have been withdrawn due to the amendment filed December 20, 2007.

Response to Arguments

4. Applicant's arguments filed on December 20, 2007, in response to the office action mailed June 22, 2007, have been fully considered and are not persuasive.

Applicant argues that Sriram et al. (Publication Number US 2002/0176489 A1) fails to teach or suggest that a buffer is inputted conditional on the next buffer being inputted **[Arguments, page 9, lines 23-25]**, that a processor is allowed to not be synchronously clocked by a sample rate **[Arguments, page**

10, lines 6-8]. For the point concerning conditional data input into buffers, the claims do not explicitly disclose that the processing of samples is in any way conditional on another action. For example, the passage in **claim 1** "*receiving samples at a third buffer during the processing of the first group of symbols*" as recited by the Applicants in the arguments could still be interpreted as samples *could* be received during processing of another group of samples *but that it is not necessarily the case* (in other words, the wording of the passage still leaves it open to the interpretation that a buffer is received during the processing of a group of samples, but that the previously mentioned group of samples could still be processed even if nothing is received at the previously mentioned buffer). If the action were indeed conditional, the proper wording for the passage would have been (again using the Applicant cited passage in the arguments) "*receiving samples at a third buffer if there is processing of the first group of symbols*" or anything of similar wording (with an emphasis on "if").

The claims further do not explicitly mention that the processor is allowed to not be synchronously clocked by a sample rate. In fact, the claim is still open to the interpretation that actions such as processing and inputting are based on a

sample rate (e.g. one group of samples is inputted at a periodic rate while another group of samples is being processed). It is noted that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicants also argue that Sriram et al. does not disclose that a specific buffer input is pointed to with each group of sample inputs. However, as seen in Figures 1 and 2, Sriram et al. discloses that there are sections that point to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1). Hence, Sriram et al. is still able to read on the claims (*see rejection under the section* ***Rejections Based on Prior Art***).

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United

States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-4, 6-7, 9-15, 17, and 22** are rejected under 35 U.S.C. 102(e) as being anticipated by Sriram et al. (Publication Number US 2002/0176489 A1).

As per **claim 1**, Sriram et al. discloses "*a method of processing digital communication signals in a system including a plurality of buffers, the method comprising: processing from all known paths of a first group of symbols* ***(time tracking that allows demodulation of a particular multipath at a particular timing condition; Page 2, paragraph 0026)***, *wherein buffered digital samples corresponding to the first group of symbols start in a first buffer and end in a second buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)***, *and receiving samples at a third buffer during the processing of the first group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***" where the buffer is circular **(Page 1, paragraph 0007)** and at each iteration the buffer "slides" by an interval of 16 chips (with each buffer consisting of 16 chips) in a circular manner to enable the datapath to have access to another

buffer **(Page 3, paragraph 0040; FIG. 2).** Since the triple buffer of the system/method is circular, Sriram et al. also discloses *"processing from all known paths of a second group of symbols, wherein buffered digital samples corresponding to the second group of symbols start in the second buffer and end in the third buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1),*** *and receiving samples at the first buffer during the processing of the second group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)"*** and *"processing from all known paths of a third group of symbols, wherein buffered digital samples corresponding to the third group of symbols start in the third buffer and end in the first buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1),*** *and receiving samples at the second buffer during the processing of the third group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009).***"

As per **claim 2**, Sriram et al. discloses "*the plurality of buffers hold a number of digital samples* ***(despread symbols dumped into a finger symbol buffer)***, *the number being adjusted for communication conditions* ***(number of despread symbols dumped into a finger symbol buffer depends on the value of SF (symbol fingers); Page 3, paragraph 0041).***"

As per **claim 3**, Sriram et al. discloses "*the communication conditions include a communication technology* ***(system/method capable of supporting spread-spectrum CDMA; Page 4, paragraph 0048)*** *and anticipated maximum useful multi-path delay in an environment* ***(system/method is capable of handling special cases of early/ontime/late correlations that occur when the on-time sample is near a chip boundary; Page 4, paragraph 0044; FIG. 4a-4c).***"

As per **claim 4**, Sriram et al. discloses "*received information relevant to a given group of transmitted symbols* ***(input buffer chips)*** *is processed in one iteration, without a need to store intermediate results for the given group of transmitted symbols* ***(despreading a plurality of triple data input buffer chips by the correlator datapath in a single processing cycle; Page 1, paragraph 0011).***"

As per **claim 6**, Sriram et al. discloses "*tuning a receiver to a first channel, storing received symbols from the first*

channel ***(receiving chip samples into the triple data input buffer (Page 1, paragraph 0010) with an input buffer associated with time tracking of a particular symbol multipath; Page 1, paragraph 0007),*** *and tuning the receiver to a second channel* ***(timing change associated with the chip samples, indicating that samples at another timing value has been inputted beforehand; Page 1, paragraph 0012).***"

As per **claim 7**, Sriram et al. discloses "*processing symbols received from the first channel during extra cycles of processing while the receiver is tuned to the second cycle* ***(in special cases when a timing change request has arrived, one extra cycle is idled to adjust for the time change before the system resumes normal operation; Page 1, paragraph 0007; Page 3, paragraph 0041).***"

As per **claim 9**, Sriram et al. discloses "*a method of processing digital communication signals in a system including a plurality of buffers, the method comprising: processing symbols corresponding to a first group of symbols to be processed and from all known paths* ***(time tracking that allows demodulation of a particular multipath at a particular timing condition; Page 2, paragraph 0026),*** *wherein the first group of symbols in a first path start in a first buffer and end in a second buffer* ***(two of the three buffers are available for processing by a correlator***

datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1), *and receiving samples at a third buffer during the processing the first group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***" where the buffer is circular **(Page 1, paragraph 0007)** and at each iteration the buffer "slides" by an interval of 16 chips (with each buffer consisting of 16 chips) in a circular manner to enable the datapath to have access to another buffer **(Page 3, paragraph 0040; FIG. 2)**. Since the triple buffer of the system/method is circular, Sriram et al. also discloses "*processing symbols corresponding to a second group of symbols to be processed and from all known paths, wherein the second group of symbols in a second path start in the second buffer and end in the third buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1),*** *and receiving samples at the first buffer during the processing of the second group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***" and "*processing symbols corresponding to a third group of symbols to be processed and from all known paths, wherein the third group of*

symbols in a third path start in the third buffer and end in the first buffer ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1),*** *and receiving samples at the second buffer during the processing of the third group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009).***"

Sriram et al. also discloses "*adapting duration time of the processing of the first, second, and third groups based on channel and signal conditions* ***(number of despread symbols dumped into a finger symbol buffer depends on the value of SF (symbol fingers); Page 3, paragraph 0041).***"

As per **claim 10**, Sriram et al. discloses "*an apparatus to process digital communication signals, the apparatus comprising: a plurality of buffers* ***(triple data buffer; Page 1, paragraph 0009)***" and "*a processing unit* ***(correlator coprocessor; Figure 7).***" Sriram et al. also discloses "*programmed memory having instructions* ***(configuration tables; Figure 7)*** *directing the processing unit* ***(correlator coprocessor through a controller)*** *to process digital samples corresponding to a group of symbols to be processed in a plurality of buffers, the digital samples starting in a first buffer of the plurality of buffers and*

ending in a second buffer of the plurality of buffers ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1).***"

Sriram et al. further discloses "*wherein the digital samples are received at a third buffer of the plurality of buffers during the processing of the digital samples* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009).***"

As per **claim 11**, Sriram et al. discloses "*comprising input and output busses* ***(data path; Figure 7)*** *operable to permit random access to the plurality of buffers during processing* ***(demodulation even when the mulipath is not constant; Page 2, paragraph 0026).***"

As per **claim 12**, Sriram et al. discloses "*symbols are processed in a different group of buffers after a process iteration is complete* ***(at each iteration, the buffer is shifted over by 16 chips; Figure 1).***"

As per **claim 13**, Sriram et al. discloses "*a method of processing digital communication signals, the method comprising: receiving a communication signal at a receiver* ***(date from Rx source into input buffers; Figure 7).***" Sriram et al. also

discloses "*communicating digital samples from the received communication signal to sample buffers* ***(signals from Rx source 0 and 1 to input buffers; Figure 7)***, *wherein the digital samples include symbols* ***(symbol despreading; Page 2, paragraph 0033)***." Sriram et al. discloses "*processing the symbols in a first group of sample buffers* ***(two of the three buffers, consisting of one group, are processed by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)*** *and receiving digital samples from the receiver at a second group of sample buffers during the processing* ***(remaining buffer, for the second group, is being written into by incoming chips; Page 1, paragraph 0009)***."

As per **claim 14**, Sriram et al. discloses "*after symbols in a symbol path are completely processed, designating sample buffers in the first group of sample buffers as being in the second group of sample buffers* ***(after the first iteration, there is a shift to the right of 16 chips, where the second group of 16 chips become part of the group of buffers accessible for processing in the next iteration k+1; Figure 1)***." Sriram et al. discloses "*designating sample buffers in the second group of sample buffers as being in the first group of sample buffers, whereby sample buffers are rotated between processing iterations*

and digital sample receiving operations ***(the buffer is circular (Page 1, paragraph 0007) and at each iteration the buffer 'slides' by an interval of 16 chips (each buffer consists of 16 chips) in a circular manner; Page 3, paragraph 0040; Figure 2).***"

As per **claim 15**, Sriram et al. discloses "*sample buffers in the first group of sample buffers designated as being in the second group of sample buffers include all the sample buffers in the first group of sample buffers* ***(after the first iteration, there is a shift to the right of 16 chips, where the second group of 16 chips become part of the group of buffers accessible for processing in the next iteration k+1; Figure 1)*** *except a sample buffer having an end of a symbol path* ***(at iteration k+1, buffers from the first iteration k that include the notation 'x' for 'on-time sample being used for despread' are not included; Figure 1).***"

As per **claim 17**, Sriram et al. discloses "*a method of processing digital communication signals in a system including a plurality of buffers, the method comprising: processing symbols corresponding to a first group of symbols to be processed and starting in a first buffer and ending in a second buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to***

Chip i+1); Figure 1), *and receiving samples at a third buffer during the processing of the first group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***" where the buffer is circular **(Page 1, paragraph 0007)** and at each iteration the buffer "slides" by an interval of 16 chips (with each buffer consisting of 16 chips) in a circular manner to enable the datapath to have access to another buffer **(Page 3, paragraph 0040; Figure 2).** Since the triple buffer of the system/method is circular, Sriram et al. also discloses "*processing symbols corresponding to a second group of symbols to be processed and starting in the second buffer and ending in the third buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1)***, *and receiving samples at the first buffer during the processing of the second group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009)***" and "*processing symbols corresponding to a third group of symbols to be processed and starting in the third buffer and ending in the first buffer* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions***

(e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1), *and receiving samples at the second buffer during the processing of the third group of symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009).***"

As per **claim 22**, Sriram et al. discloses "*an apparatus to process digital communication signals, the apparatus comprising: a plurality of buffers* ***(triple data buffer; Page 1, paragraph 0009)***" and "*a processing unit* ***(correlator coprocessor; Figure 7).***" Sriram et al. also discloses "*programmed memory having instructions* ***(configuration tables; Figure 7)*** *directing the processing unit* ***(correlator coprocessor through a controller)*** *to process digital samples corresponding to a group of symbols to be processed in a plurality of buffers, the digital samples starting in a first buffer of the plurality of buffers and ending in a second buffer of the plurality of buffers* ***(two of the three buffers are available for processing by a correlator datapath (Page 1, paragraph 0009), with sections pointing to specific portions (e.g. PNi points to Chip i and PNi+1 points to Chip i+1); Figure 1).***"

Sriram et al. further discloses "*the digital samples are received at a third buffer of the plurality of buffers during the processing of the digital samples* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009),*** *and*

wherein the processing unit ***(through a correlator datapath)*** *is operable to select digital samples or an intermediate result from a buffer coupled to the processing unit* ***(despreading a plurality of triple data input buffer chips selected from two buffers available for processing; Page 1, paragraph 0011)***."

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram et al. (Publication Number US 2002/0176489 A1) in view of Lee et al. (Patent Number US 6,650,140 B2)

As per **claim 5**, Sriram et al. discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Though Sriam et al. discloses "*process received symbols in the plurality of buffers* ***(despreading a plurality of triple data input buffer chips selected from two buffers; Page 1, paragraph 0011),***" Sriram et

al. does not disclose "*turning off a receiver subsystem and continuing to process received symbols in the plurality of buffers.*"

Lee et al. discloses "*turning off a receiver subsystem and continuing to process received symbols in the plurality of buffers* ***(receiver can be turned off if it is not needed; Column 15, lines 40-44).***"

Sriram et al. and Lee et al. are analogous art in that they are from the same field of communication systems and interfacing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method of processing digital communication signals in a system including a plurality of buffers as disclosed by Sriram et al. with the idea of the turning off the receiver as disclosed by Lee et al., which Lee et al. notes is related to a power-down mode **(Column 15, lines 40-41).** The ability to power down any unused components can allow a device to save power, especially in mobile devices that run off a battery with a finite amount of power.

9. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram et al. (Publication Number US

2002/0176489 A1) in view of Kim et al. (Patent Number US 6,714,527 B2).

As per **claim 8**, Sriram et al. discloses "*the method*" (*see rejection to* ***claim 1*** *above*). However, Sriram et al. does not explicitly disclose "*the first, second, and third paths have different sampling rates.*"

Kim et al. discloses "*a first, second, and third paths have different sampling rates* ***(a plurality of communication signals have differing spreading codes; Abstract, lines 1-2).***"

Sriram et al. and Kim et al. are analogous art in that they are from the same field of communication systems, particularly regarding the CDMA protocol.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method of processing digital communication signals in a system including a plurality of buffers as disclosed by Sriram et al. with the idea of the paths have different sampling rates as disclosed by Kim et al.

Kim et al. notes that using a plurality of spreading codes, with each code pertaining to a particular user, would allow a signal from a particular user relating to a particular spreading code to be enhanced while the signals for other users are not enhanced **(Column 1, lines 60-65)**. This is particularly useful in

multiple access digital communication systems, where a plurality of users can access the same communication medium to transmit or receive data **(Column 1, lines 15-21),** with such systems being useful within communication media with limited bandwidth.

10. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram et al. (Publication Number US 2002/0176489 A1) in view of Roohparvar (Patent Number US 6,615,307 B1).

As per **claim 16**, Sriram et al. discloses "*the method*" (*see rejection to **claim 13** above*). However, Sriram et al. does not disclose "*shutting down sample buffers when sufficient processing is complete.*"

Roohparvar "*shutting down sample buffers **(input buffers)** when sufficient processing is complete **(during power-down modes, which shows that there are no further processes to handle; Column 5, lines 6-8)**.*"

Sriram et al. and Roohparvar are analogous art in that they are from the same field of interface buffering.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method of processing digital communication signals in a system including a plurality of buffers as disclosed by Sriram et al. with the idea of the turning off the buffers as disclosed by Roohparvar, which

Roohparvar notes is related to providing low standby power **(Column 5, lines 6-8)**. The ability to power down any unused components can allow a device to save power, especially in mobile devices that run off a battery with a finite amount of power.

11. **Claims 18-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram et al. (Publication Number US 2002/0176489 A1) in view of Robertson et al. (Publication Number US 2001/0038633 A1).

As per **claim 18**, Sriram et al. discloses "*a method of processing digital communication signals in a system including a plurality of buffers, the method comprising: processing from all known paths of a first group of symbols* ***(time tracking that allows demodulation of a particular multipath at a particular timing condition; Page 2, paragraph 0026)***" and the idea of processing data from certain buffers while receiving samples at other buffers in "*wherein buffered digital samples corresponding to the first group of symbols start in a first buffer and end in a third buffer, and receiving samples at a fourth buffer and a fifth buffer during the processing of the first group of symbols* ***(two of the three buffers are available for processing by a correlator datapath while the remaining buffer is being written into by incoming chips; Page 1, paragraph 0009),***" where the

buffer is circular **(Page 1, paragraph 0007)** and at each iteration the buffer "slides" by an interval of 16 chips (with each buffer consisting of 16 chips) in a circular manner to enable the datapath to have access to another buffer **(Page 3, paragraph 0040; Figure 2).**

However, Sriram et al. does not disclose the use of five buffers as noted in "*processing from all known paths of a second group of symbols, wherein buffered digital samples corresponding to the second group of symbols start in the third buffer and end in the fifth buffer, and receiving samples at the first buffer and second buffer during the processing of the second group of symbols,*" "*processing from all known paths of a third group of symbols, wherein buffered digital samples corresponding to the third group of symbols start in the fifth buffer and end in the first buffer, and receiving samples at the fourth buffer and the third buffer during the processing of the third group of symbols,*" "*processing from all known paths of a fourth group of symbols, wherein buffered digital samples corresponding to the fourth group of symbols start in the first buffer and end in the third buffer, and receiving samples at a second buffer and the fifth buffer during the processing of the fourth group of symbols*" "*processing from all known paths of a fifth group of symbols, wherein buffered digital samples corresponding to the*

fifth group of symbols start in the third buffer and end in the fifth buffer, and receiving samples at the fourth buffer and the first buffer during the processing of the fifth group of symbols," and "*processing from all known paths of a sixth group of symbols, wherein buffered digital samples corresponding to the sixth group of symbols start in the fifth buffer and end in the first buffer, and receiving samples at the second buffer and the first buffer during the processing of the sixth group of symbols.*"

Robertson et al. discloses the use of a buffer with five entries **(Page 9, paragraph 0077),** which combined with the buffering system of Sriram et al. discloses "*processing from all known paths of a second group of symbols, wherein buffered digital samples corresponding to the symbols start in the third buffer and end in the fifth buffer* ***(several of the buffers are available for processing by a correlator datapath),*** *and receiving samples at the first buffer and second buffer during the processing of the symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009),***" "*processing from all known paths of a third group of symbols, wherein buffered digital samples corresponding to the symbols start in the fifth buffer and end in the first buffer* ***(several of the buffers are available for processing by a correlator datapath),***

and receiving samples at the fourth buffer and the third buffer during the processing of the symbols ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009),*** *"processing from all known paths of a fourth group of symbols, wherein buffered digital samples corresponding to the symbols start in the first buffer and end in the third buffer* ***(several of the buffers are available for processing by a correlator datapath),*** *and receiving samples at a second buffer and the fifth buffer during the processing of the symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009),"*** *"processing from all known paths of a fifth group of symbols, wherein buffered digital samples corresponding to the symbols start in the third buffer and end in the fifth buffer* ***(several of the buffers are available for processing by a correlator datapath),*** *and receiving samples at the fourth buffer and the first buffer during the processing of the symbols* ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009),"*** and *"processing from all known paths of a sixth group of symbols, wherein buffered digital samples corresponding to the symbols start in the fifth buffer and end in the first buffer* ***(several of the buffers are available for processing by a correlator datapath),*** *and receiving samples at the second buffer and the first buffer during the processing of*

the symbols ***(remaining buffer is being written into by incoming chips; Page 1, paragraph 0009).***"

Sriram et al. and Robertson et al. are analogous art in that they focus on the problem of buffering within a communication system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the method of processing digital communication signals in a system including a plurality of buffers as disclosed by Sriram et al. with the idea of the using a five-entry buffer as disclosed by Robertson et al.

Robertson et al. notes that it is prudent to include at least one more additional entry in several cases, notably where the receive clock is faster than the transmit clock and to account for maximum phase skew that may be present between transmit and receive clocks **(Page 9, paragraph 0077).** Having five entries as opposed to three entries in a buffer not only can better account for the rate discrepancy between the system's receiver and a separate system's transmitter, but also can allow for more data to be stored before processing.

As per **claim 19**, the combination of Sriram et al. and Robertson et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Sriram et al. further discloses "*each of the*

plurality of buffers holds a different number of digital samples ***(despread symbols dumped into a finger symbol buffer)*** *based on communication conditions* ***(number of despread symbols dumped into a finger symbol buffer depends on the value of SF (symbol fingers); Page 3, paragraph 0041).***"

As per **claim 20**, the combination of Sriram et al. and Robertson et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Sriram et al. further discloses "*the communication conditions include multi-path delays* ***(system/method is capable of handling special cases of early/ontime/late correlations that occur when the on-time sample is near a chip boundary; Page 4, paragraph 0044; Figure 4a-4c)*** *and waveform features* ***(data portions are associated with time tracking of a particular symbol multipath; Page 2, paragraph 0033).***"

As per **claim 21**, the combination of Sriram et al. and Robertson et al. discloses "*the method*" (*see rejection to* ***claim 18*** *above*). Sriram et al. further discloses "*the paths are from a plurality of base stations* ***(the system is capable of performing CDMA base station operations (Page 4, paragraph 0048) in a multipath environment that may not be constant; Page 2, paragraph 0026).***"

RELEVENT ART CITED BY THE EXAMINER

12. The following prior art made of record and relied upon is citied to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c).**

13. The following references teach data transfer as they pertain to IC circuits, especially in the setting and transfer of data/parameters.

U.S. PATENT NUMBERS:

5,864,714

5,892,980

CONCLUDING REMARKS

Conclusions

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action

is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HENRY YU whose telephone number is (571)272-9779. The examiner can normally be reached on Monday to Friday, 8:00 AM to 5:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. Y./
Examiner, Art Unit 2182

/Henry W.H. Tsai/
Supervisory Patent Examiner, Art Unit 2184